Claims

[c1] 1.An integrated circuit structure comprising:
a substrate having at least two types of crystalline orientations;
first-type transistors formed on first portions of said substrate having a first type of crystalline orientation;
second-type transistors formed on second portions of said substrate having a second type of crystalline orientation; and
a straining layer above said first-type transistors and said second-type transistors.

[c2] 2.The structure in claim 1, wherein said first-type transistors and said second-type transistors include silicide regions and said straining layer is above said silicide regions.

[c3] 3.The structure in claim 2, wherein said first-type transistors and said second-type transistors include source and drain regions formed within said substrate and a gate conductor formed over said substrate between said source and drain regions, and
wherein said silicide regions are formed over said gate conductor and said source and drain regions.

[c4] 4.The structure in claim 1, wherein said first-type transistors are complementary to said second-type transistors.

[c5] 5. The structure in claim 1, wherein said first portions of said substrate comprise non-floating substrate portions and said second portions of said substrate comprise floating substrate portions.

[c6] 6.The structure in claim 1, wherein said straining layer is strained above said first-type transistors and is relaxed above said second-type transistors.

[c7] 7.The structure in claim 1, wherein said first-type transistors and said second-type transistors comprise one of planar complementary metal oxide semiconductor (CMOS) transistors and fin-type field effect transistors (FinFETs).

[c8] 8.An integrated circuit structure comprising:
a substrate having at least two types of crystalline orientations;
N-type field effect transistors (NFETs) formed on first portions of said substrate having a first type of crystalline orientation;
P-type field effect transistors (PFETs) formed on second portions of said substrate having a second type of crys-

talline orientation; and
a straining layer above said NFETs and said PFETs.

[c9] 9.The structure in claim 8, wherein said NFETs and said PFETs include silicide regions and said straining layer is above said silicide regions.

[c10] 10.The structure in claim 9, wherein said NFETs and said PFETs include source and drain regions formed within said substrate and a gate conductor formed over said substrate between said source and drain regions, and wherein said silicide regions are formed over said gate conductor and said source and drain regions.

[c11] 11.The structure in claim 8, wherein said NFETs are complementary to said PFETs.

[c12] 12. The structure in claim 8, wherein said first portions of said substrate comprise non-floating substrate portions and said second portions of said substrate comprise floating substrate portions.

[c13] 13.The structure in claim 8, wherein said straining layer is strained above said NFETs (N-type) and is relaxed above said PFETs.

[c14] 14.The structure in claim 8, wherein said NFETs and said PFETs comprise one of planar complementary metal ox-

ide semiconductor (CMOS) transistors and fin-type field effect transistors (FinFETs).

[c15] 15.A method of forming an integrated circuit structure, said method comprising:
bonding a first substrate structure on a second substrate structure to form a laminated structure having a first substrate with a first crystalline orientation above a second substrate with a second crystalline orientation;
etching first openings in said laminated structure down to said second substrate;
growing additional material on said second substrate to fill said first openings to produce a substrate at the top of said laminated structure that has first portions having said first type of crystalline orientation and second portions having said second type of crystalline orientation;
forming first-type transistors above said first portions of said substrate;
forming second-type transistors above said second portions of said substrate; and
forming a straining layer above said first-type transistors and said second-type transistors.

[c16] 16.The method in claim 15, further comprising forming silicide regions on said first-type transistors and said second-type transistors, wherein said straining layer is formed above said silicide regions.

[c17] 17.The method in claim 16, wherein said forming of said first-type transistors and said forming of said second-type transistors comprises forming source and drain regions within said substrate and a gate conductor over said substrate between said source and drain regions, wherein said silicide regions are formed over said gate conductor and said source and drain regions.

[c18] 18.The method in claim 15, wherein said first-type transistors are complementary to said second-type transistors.

[c19] 19. The method in claim 15, further comprising relaxing strain in portions of said straining layer that are above said second-type transistors.

[c20] 20.The method in claim 15, wherein said first-type transistors and said second-type transistors comprise one of planar complementary metal oxide semiconductor (CMOS) transistors and fin-type field effect transistors (FinFETs).